Intel® E7221 Chipset

Specification Update

For the Intel® E7221 Memory Controller Hub (MCH)

September 2004

Notice: The Intel® E7221 MCH may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

Document Number: 303631-001

Contents

Revision History

Revision	Description	Date
001	Initial Release	September 2004

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Preface

This document is an update to the specifications contained in the documents listed in the following Affected Documents table. It is a compilation of device and document errata and specification clarifications and changes, and is intended for hardware system manufacturers and for software developers of applications, operating system, and tools.

Information types defined in the Nomenclature section of this document are consolidated into this update document and are no longer published in other documents. This document may also contain information that has not been previously published.

Affected Documents

Document Title	Document Number
Intel® E7221 Chipset Datasheet	303630-001

Nomenclature

Errata are design defects or errors. Errata may cause the Intel® E7221 Chipset's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Component Identification Information

The Intel E7221 MCH may be identified by the following register contents:

Stepping	Vendor ID[1]	Device ID[2]	Revision Number[3]
B2	8086h	2588h	05h

NOTES:
1. The Vendor ID corresponds to bits 15:0 of the Vendor ID Register located at offset 00–01h in the PCI function 0 configuration space.
2. The Device ID corresponds to bits 15:0 of the Device ID Register located at offset 02–03h in the PCI function 0 configuration space.
3. The Revision Number corresponds to bits 7:0 of the Revision ID Register located at offset 08h in the PCI function 0 configuration space.

Component Marking Information

The Intel E7221 MCH may be identified by the following component markings:

Stepping	S-Spec	Top Marking	Notes
B2	SL7YQ	NG88CUR	Production Samples

Summary Tables of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes that apply to the listed component steppings. Intel intends to fix some of the errata in a future stepping of the component, and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X: Erratum, Specification Change or Clarification that applies to this stepping.

(No mark) or (Blank Box): This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Status

Doc: Document change or update that will be implemented.

PlanFix: This erratum may be fixed in a future stepping of the product.

Fixed: This erratum has been previously fixed.

NoFix: There are no plans to fix this erratum.

Shaded: This item is either new or modified from the previous version of the document.

NO.	B2	PLANS	ERRATA
1	X	NoFix	Incorrect PCI Express* Lane Transition after Receiving Several TS1 Packets
2	X	NoFix	MCH Does Not Ignore A PCI Express Null Packet
3	X	NoFix	Data Payload Byte Count Supplied During An Unsupported Upstream Configuration Read Is Not 4 Bytes
4	X	NoFix	PCI Express Replay Timer Register Default Setting Is Incorrect
5	X	NoFix	PCI Express Common Mode Voltage Noise Immediately Following Receiver Detect Sequence
6	X	NoFix	DMI Link Egress Port Address is Not Programmable
7	X	NoFix	MCH Does Not Send Minimum Number TS2 on PCI Express
8	X	NoFix	DMI Traffic Ordering Violation
9	X	NoFix	The E_SMERR bit May be Incorrectly Set When Performing Valid Access to SMM Space
10	X	NoFix	DDR2-533 Duty Cycle

NO.	SPECIFICATION CHANGES
1	CID (Component Identification) and TCID (Target Component Identification) fields in all tree elements of the MCH topology are not always mirrors of each other.
2	The MCH is limited to reporting Poisoned TLPs through standard PCI error status reporting structures.

NO.	SPECIFICATION CLARIFICATIONS
	There are no specification clarifications.

NO.	DOCUMENTATION CHANGES
	There are no documentation changes.

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Errata

1. Incorrect PCI Express Lane Transition after Receiving Several TS1 Packets

Problem: If MCH receives several TS1 packets with Link and Lane numbers set to PAD, after 4 µs it will time out and transition into configuration state instead of going directly to the Detect state as it should. However, the link will still transition to the Detect state after timing out of Configuration.

Implication: The MCH will experience longer latency when transitioning to Detect state.

Workaround: None at this time.

Status: Closed. For affected steppings, see the *Summary Table of Changes*.

2. MCH Does Not Ignore a PCI Express Null Packet

Problem: If the MCH receives a PCI Express Null packet, it should drop the packet and not perform sequence number checking or respond with any Ack or Nak DLLP. The issue is that the MCH still performs sequence number checks for Null packets and may respond with an ACK or NAK depending on the result of the check.

Implication: MCH may send ACK or NAK DLLPs in response to a Null packet. This may degrade link performance due to unnecessary retries.

Workaround: None at this time.

Status: Closed.

3. Data Payload Byte Count Supplied during An Unsupported Upstream Configuration Read Is Not 4 Bytes

Problem: During configuration reads to unsupported PCI Express configuration space, the byte count for data payload is not 4.

Implication: Data payload byte count is 5 and not the expected 4.

Workaround: Closed. Do not perform unsupported upstream PCI Express configuration cycles.

Status: Closed.

4. PCI Express Replay Timer Register Default Setting Is Incorrect

Problem: Replay will occur 100 symbol times sooner than expected.

Implication: Retrain of the link may occur more often with devices that have slower ACK to packets from the MCH.

Workaround: BIOS will need to reprogram the Replay Timer Register to reflect actual exit latency value. Contact your Intel Field Representative for the latest BIOS information.

Status: Closed. For affected steppings, see the *Summary Table of Changes*.

5. PCI Express Common Mode Voltage Noise Immediately following Receiver Detect Sequence

Problem: The PCI Express Common Mode Voltage is not stable immediately after Receiver Detect Sequence when entering Polling.Active from Detect.Active states.

Implication: Common Mode Voltage noise may result in bit errors early in Polling.Active state. May result in additional training time before transitioning on to Polling.Configuration.

Workaround: None at this time.

Status: Closed. For affected steppings, see the *Summary Table of Changes*.

6. DMI Link Egress Port Address Is Not Programmable

Problem: The PCI SIG approved ECR 04 to allow future system software (e.g., Operating System) to discover the link structure of the Root Complex. One of the registers in the MCH that "points" from the DMI port to the ICH6 cannot be programmed correctly.

Implication: There is no impact on platform functionality. ECR's do not retroactively apply to the current PCI Express 1.0a specification, and no existing software understands the Root Topology discovery structures. These structures are implemented in the MCH only to aid future software development. Such software will need to comprehend the incorrect pointer.

Workaround: None at this time.

Status: Closed. For affected steppings, see the *Summary Table of Changes*.

7. MCH Does Not Send Minimum Number TS2 on PCI Express

Problem: On PCI Express the MCH transitions to Recovery. Idle after sending 9 TS2s after receiving the 1st TS2 from the endpoint. The PCI Express specification requires that a device send a minimum of 16 TS2s after detecting the first TS2.

Implication: If the endpoint is unable to consecutively receive 8 of the 9 transmitted TS2s, a 48 ms timeout will be incurred before the device transitions to Detect state and re-attempt training. All known production devices have been able to properly train after receiving 9 TS2s.

Workaround: None at this time.

Status: Closed. For affected steppings, see the *Summary Table of Changes*.

8. DMI Traffic Ordering Violation

Problem: Under certain traffic scenarios including AC97 and USB it is possible for upstream data on the DMI link to violate ordering rules. For example, a read completion to the CPU may be allowed to pass a prior write to memory.

Implication: The ordering violation may result in a system hang or unpredictable system behavior.

Workaround: Contact your Intel Field Representative for the latest BIOS information.

Status: Closed. For affected steppings, see the *Summary Table of Changes*.

9. The E_SMERR Bit May be Incorrectly Set When Performing Valid Accesses to SMM Space

Problem: The E_SMERR bit may be incorrectly set when performing valid accesses to SMM space

Implication: If this bit is used by the SMI handler to determine cache line flushes, unnecessary cache line flushes may occur when in SMM mode. A slight performance impact to the SMI handler may result from unnecessary cache line flushes.

Workaround: None at this time.

Status: Closed. For affected steppings, see the *Summary Table of Changes*.

10. DDR2-533 Duty Cycle

Problem: When using internal graphics and system memory is DDR2-533, the differential clocks do not meet minimum period of 3.75 nsec and duty cycle of 45/55%, as specified by JEDEC. The measured duty cycle is 44/56%. The duty cycle is within specification when using external graphics or DDR2-400.

Implication: Intel has characterized the system memory clocks and shared the data with the major DRAM suppliers. Intel and the major DRAM suppliers agree that this system clock erratum should not cause system clock related timing issues providing all other DRAM related interface timing specifications are fulfilled according to Intel DDR2 specification addendum. Intel determined that the worst case minimum clock period of 3.55 nsec does not occur on consecutive clock pulses.

Workaround: None at this time.

Status: Closed. For affected steppings, see the *Summary Table of Changes*.

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Specification Changes

1. CID (Component Identification) and TCID (Target Component Identification) fields in all tree elements of the MCH topology are not always mirrors of each other.

Problem: CID and TCID fields in all tree elements of the MCH topology are not always mirrors of each other.

Implication: BIOS will need to program all TCID and CID tree element registers, instead of relying on default values.

Workaround: BIOS now must program all tree elements when it programs any one.

Status: Closed.

2. The MCH is limited to reporting Poisoned TLPs through standard PCI error status reporting structures

Problem: The MCH does not set the Non-Fatal Error Detected status bit, in the PCI Express Device Status register when a poisoned TLP is received

Implication: Future OS's (that comprehend PCI Express error reporting) will not be notified via standard PCI Express mechanisms when a poisoned TLP is received.

Workaround: Standard PCI error status reporting must be used for Poisoned TLP reporting. The reception of Poisoned TLP is reported by hardware setting the Detected Parity Error bit in Device 1, secondary status register, and if so enabled by additionally setting the Master Data Parity Error bit in the same register.

Status: Closed.

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Specification Clarifications

There are no specification clarifications in this Specification Update revision.

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Documentation Changes

There are no documentation changes in this Specification Update revision.

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